**Computer Organization and Architecture**

**(21ECSC201)**

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**Activity Report**

**Course details**

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| **Course Name** | Computer Organization and Architecture |
| **Course Code** | 21ECSC201 |
| **Semester** | III |
| **Division** | C |
| **Year** | 2023-24 |

**Team Details**

**Group No: C1\_8**

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1. **Problem Statement**

**The need statement given to us was to design a 16 bit processor with 3 address format and direct addressing mode**

1. **Brief description of the functional specifications of the Processor designed**

**The design of a 16-bit processor with a 3-address format and direct addressing mode involves several functional specifications to meet the requirements. Below is a brief description of the key functional specifications for such a processor:**

**16-Bit Architecture:**

**The processor operates on a 16-bit architecture, meaning that it processes data in 16-bit chunks. This allows for a wide range of data representation and manipulation.**

**3-Address Format:**

**The processor supports a 3-address instruction format, where each instruction includes three operand addresses. This format provides flexibility in performing complex arithmetic and logical operations, as each instruction can involve three separate operands.**

**Direct Addressing Mode:**

**The processor incorporates a direct addressing mode, allowing instructions to specify the memory address directly as an operand. This mode simplifies memory access by directly pointing to the location where data or instructions are stored.**

**Register File:**

**The processor includes a set of registers for efficient data storage and manipulation. These registers are used as operands in instructions, allowing for quick access and manipulation of data without the need to access memory frequently.**

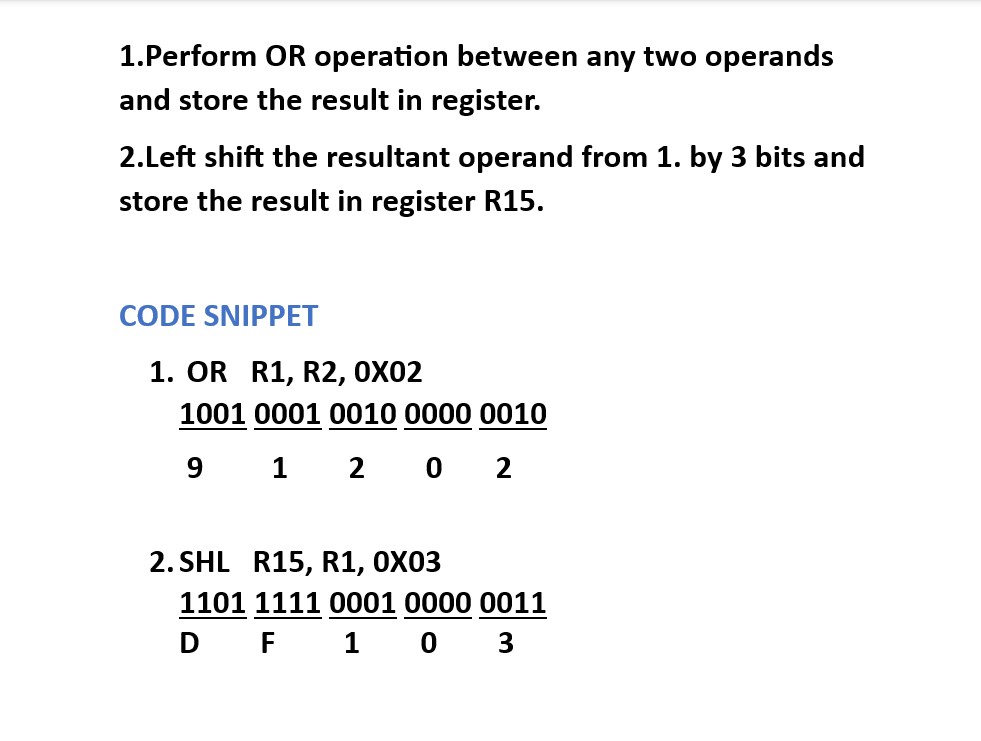
**ALU (Arithmetic Logic Unit):**

**The processor is equipped with an ALU capable of performing a range of arithmetic and logical operations on the data stored in registers or memory. The ALU supports the 3-address format, allowing it to operate on three operands simultaneously.**

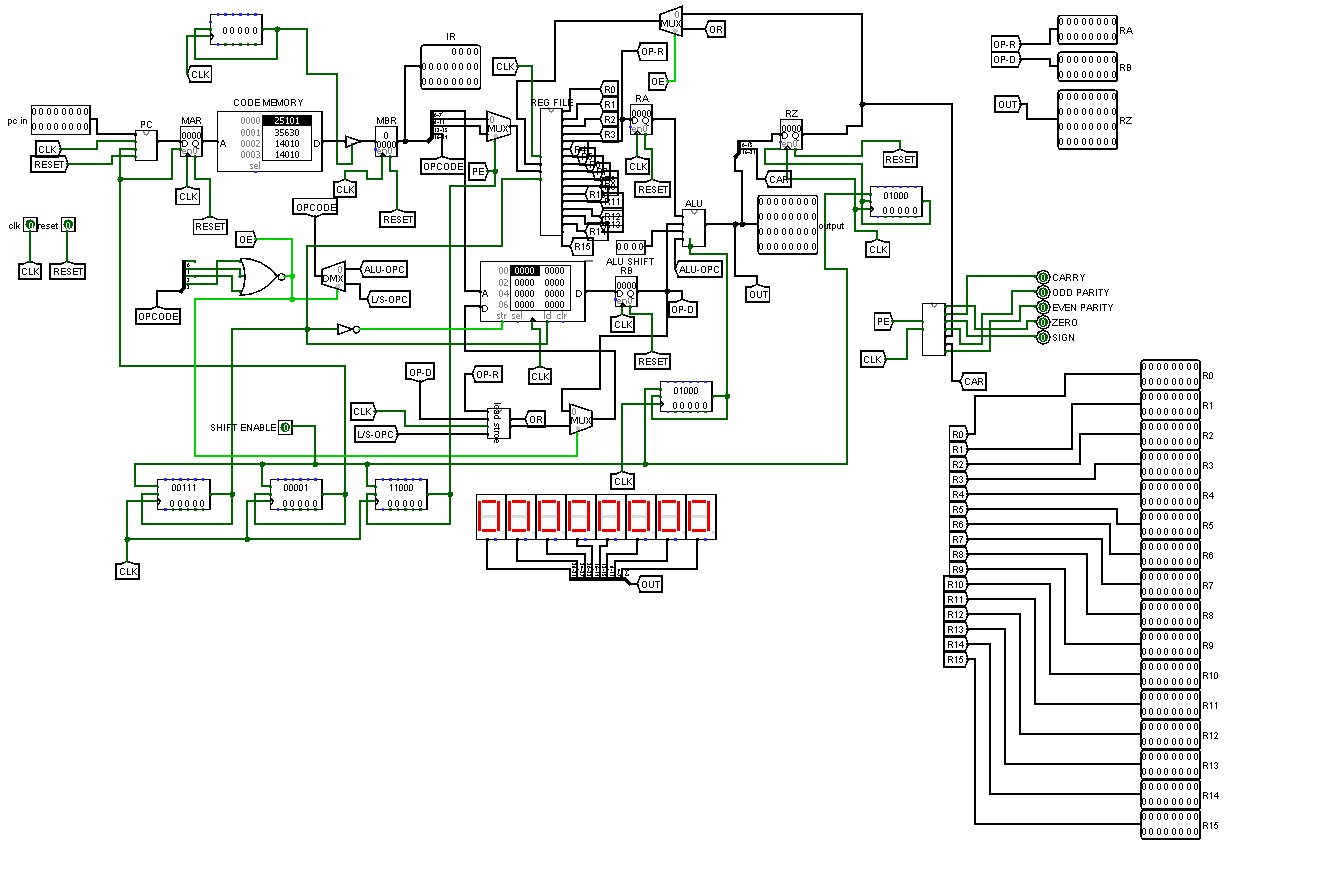
**Pipeline Architecture:**

**To enhance performance, the processor employs a pipeline architecture. This allows multiple instructions to be in different stages of execution simultaneously, improving throughput and overall processing speed.**

**3. Code snippet executed on the machine**



**4. Processor Design**



**5. Challenges Faced**

**During the course of this project, our team of 4 members faced a lot of challenges. The challenges encountered during the project underscored the complexities associated with building a 2-stage pipeline. Coordinating the flow of data between stages, especially during the loading, storing and exchanging processes, presented intricate hurdles that required careful consideration. Additionally, the team grappled with the intricacies of maintaining the Program Status Word (PSW), a critical component for tracking the state and condition of the processor. Navigating through these challenges demanded collaborative problem-solving and a deep understanding of the pipeline architecture. Despite the difficulties, the team's collective effort and perseverance ultimately led to valuable insights and successful resolution of these issues, contributing to the overall growth and learning experience of the project.**

**6. How you overcame those challenges**

**To overcome the challenges faced during the project, we implemented a collaborative and systematic approach. For addressing the complexities of building a 2-stage pipeline, we conducted thorough discussions and leveraged each team member's expertise to design an efficient pipeline architecture. Regular brainstorming sessions allowed us to identify potential bottlenecks and streamline the flow of data between pipeline stages.**

**Dealing with the intricacies of loading, storing, and exchanging data required a meticulous examination of the data handling mechanisms. We implemented optimized algorithms and fine-tuned the data transfer processes to enhance efficiency. This involved refining memory management techniques and ensuring seamless communication between pipeline stages.**

**Maintaining the Program Status Word (PSW) demanded careful attention to detail. We established comprehensive error-checking mechanisms and implemented rigorous testing procedures to monitor and adjust the PSW accurately.**

**Throughout these challenges, effective communication within the team played a pivotal role. Sharing insights, troubleshooting collectively, and learning from each other's experiences fostered a collaborative environment.**

**7.** **Brief Comparative study of contemporary processors**

**Contemporary processors, also known as modern microprocessors, have undergone significant advancements to meet the escalating demands of computing applications. One notable trend is the move towards multi-core architectures, where processors integrate multiple processing units on a single chip. This design enables parallel processing, enhancing overall performance and efficiency.**

**The evolution of instruction set architectures (ISA) has also been a focal point. Contemporary processors support complex and diverse instruction sets, catering to a wide array of applications from general-purpose computing to specialized tasks like artificial intelligence and machine learning.**

**Power efficiency and sustainability have become critical considerations in contemporary processor design. Dynamic Voltage and Frequency Scaling (DVFS) techniques allow processors to adjust their power consumption based on workload demands, optimizing energy usage. Security features have gained prominence to address the growing concerns about cybersecurity.**

**The era of cloud computing has influenced processor design, with an emphasis on scalability and virtualization support. Processors are designed to efficiently handle virtualized workloads, ensuring seamless operation in cloud environments where resource allocation and dynamic workload management are crucial.**

**In summary, contemporary processors reflect a dynamic landscape characterized by multi-core architectures, advanced manufacturing processes, diverse instruction sets, increased power efficiency, enhanced security features, and adaptability to the demands of cloud computing and emerging technologies. This continuous evolution is driven by the need for faster, more efficient, and versatile computing solutions in our increasingly interconnected and data-driven world.**

**8. Conclusion**

**So, this was a wonderful project given to us to design a 16 bit processor with 3 address format and direct addressing mode. We as a team learnt a lot of new and creative ideas to complete the project. Collaborative projects like these often provide teams with the opportunity to apply theoretical knowledge in a practical setting, fostering creativity and problem-solving skills.**

**Throughout the project, our team likely gained insights into the intricacies of processor architecture, instruction set design, addressing modes, and the challenges associated with creating a functional and efficient system. Moreover, working on such projects enhances teamwork, communication, and project management skills as team members collaborate to achieve a common goal.**

**The learning experience likely extended beyond the technical aspects, encompassing project planning, documentation, testing methodologies, and the importance of clear communication within the team. As you reflect on the project, consider documenting the key lessons learned, both in terms of technical skills and teamwork dynamics, as this can be valuable for future endeavors.**

**Completing a project of this nature is a significant achievement and we have gained valuable knowledge in the academic and professional pursuits.**